Scanning SQUID Microscopy for Die Level Fault Isolation

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Abstract

This paper presents detailed results of scanning SQUID microscopy (SSM) analyses performed on the frontside and backside of both loose and packaged die. Optical and SEM images of localized defects are shown. Comparisons with alternative physical fault isolation (PFI) techniques like liquid crystal (LC), Schlieren thermal mapping (STM), temperature induced voltage alteration (TIVA), and photon emission microscopy (PEM) are included. Finally, limitations with and potential improvements for die level SSM are also discussed.

Introduction

Scanning SQUID (superconducting quantum interference device) microscopy has been well documented for two-dimensional current density imaging in microelectronic devices [1]-[3]. A number of publications describe its specific use for IC packaging failures [4]-[8]. Of added interest is the utility of SSM for isolation of short circuit defects within the silicon die itself. Publications having specific mention of die level SSM are limited in detail [9]-[11].

Two attributes of SSM make it attractive for die level imaging of current density. The first is the nature of magnetic flux to pass through non-ferrous materials undisturbed (notwithstanding the decrease in field strength with distance), enabling non-destructive measurement at die surfaces with minimal sample preparation. Intervening package materials, interconnect wiring, or silicon substrates that may obstruct signals with other PFI methods are not an impediment.

The second is the wide dynamic range and low-end sensitivity of the SQUID. This allows imaging in situations where other techniques may be limited - specifically large area defects with very low resistance. Here low power density and large heat diffusion may obviate thermal analysis. Such samples are also difficult to bias at energies sufficient to effect photon emission.

The results of four separate analyses follow. All SSM data were taken using a high-temperature superconductor (HTS) scanning SQUID microscope with a Z-oriented (i.e., planar to the sample surface) SQUID operating at 70-73K. SQUID-to-sample separation was in the range of just under 100 to about 600 microns. Devices were stimulated using a sinusoidal AC voltage at 9.5 kHz, with a DC offset of one-half of the peak-to-peak voltage to maintain a positive bias. The frequency was chosen arbitrarily to be in the approximate center of the SQUID electronics bandwidth. Bias was applied in two-point mode from V_{DD} to ground with all other pins floating. The peak voltage was selected to provide enough current for a reasonable signal-to-noise ratio without exceeding specified operating voltage limits.

A lock-in amplifier synchronized with the stimulus frequency was used to minimize the influence of background flux caused by ferrous materials and other DC fields, and asynchronous currents. Typical scan times were 45 minutes, not including setup and data analysis. Raw magnetic flux gradients were automatically transformed to current density using a fast-Fourier transform (FFT) inversion [12]. Data were further post-processed using commercial image analysis software to highlight gradients with false-color mapping, to overlay current density with optical and CAD layout images, and to produce three-dimensional surface plots.

Static RAM Standby Current Failure

A 10 x 14 mm, 0.4 micron L-drawn, four-level metal, 4 MB SRAM having high standby current at wafer test was examined by SSM, LC, PEM, and TIVA. The purpose of the analysis was to determine the capability of SSM for die level fault isolation and to compare it to known alternatives. LC analysis was performed from the frontside of the die, after which it was flip-chip mounted on a ceramic ball-grid array (CBGA) substrate, thinned to approximately 70 microns of remaining silicon, and optically polished. It was then analyzed from the backside by SSM, PEM, and TIVA.

The device was scanned while in a surface mount socket on a tester interface board, biased at 130 $mVAC_{pp}$ drawing 100 μA (DC average power P_{eff}

= 6.4 μW). The results are shown in Figure 1a, where the highlighted peak corresponds with the LC location observed from the frontside of the die prior to packaging, seen at the arrow in the inset. PEM analysis on the same device at 2.0 VDC with 200 mA, and TIVA at 5mA, are shown for comparison in Figure 1b.

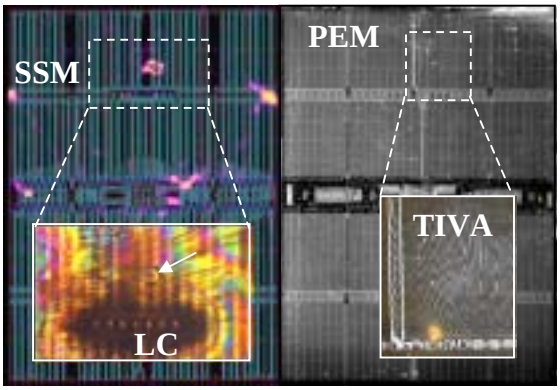

Figure 1: a) SSM and LC results for standby current failure on a 10x14 mm SRAM. b) PEM and TIVA images.

ASIC Burn-in Failure

Power supply shorts on a 9 mm square, 0.16 micron L-drawn ASIC test site, caused by electrical overloads during burn-in, were found optically after etching to silicon level (frontside liquid crystal was unsuccessful). Figure 2 shows an optical image of a typical shorting site at silicon level in a 990 micron wide by 0.6 micron long NFET in a power supply isolation device. There are ten identical instances of the overload-sensitive circuit on the chip, outlined in Figure 3.

Figure 2: Optical image of typical NFET overload site at silicon level.

A flip-chip CBGA-packaged device, thinned to 180 microns, was scanned with SSM to determine its ability to locate the low resistance shorts where liquid crystal had failed. The device was biased at 60 $mVAC_{PP}$ and drew 10 mA (P_{eff} = 300 μW). The resulting current density is overlaid with a backside near-infrared (NIR) optical image in Figure 4a. Figure 4b shows the result of thresholding the peak current density at location 'F', highlighted in Fig. 4a, to one 20 x 25 micron pixel. TIVA results from the same device are seen in Figure 5 for comparison, indicating good agreement with five of the six SSM sites identified.

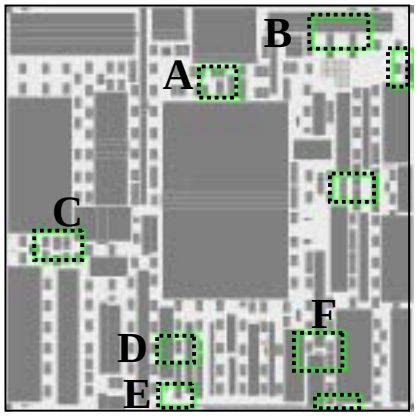

Figure 3: Locations of potential overload-sensitive circuits.

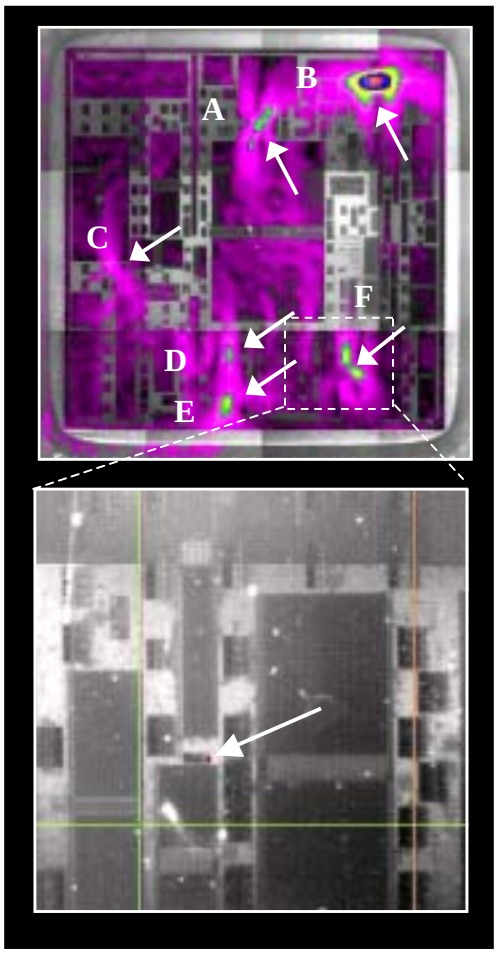

Figure 4: a) SSM signal overlaid with backside optical image on a 9 mm-square ASIC test site. b) Thresholded SSM signal from location 'F'.

The prominent current density peak noted at location 'B' in Fig. 4a is shown magnified in Figure 6a, and overlaid with CAD layout data. The

arrows indicate current paths in the last metal power busses consistent with the polarity and intensity of the magnetic flux measured. A surface plot of the same peak is seen in Figure 6b, showing the peaked nature of the SSM signal and greater detail in the surrounding data.

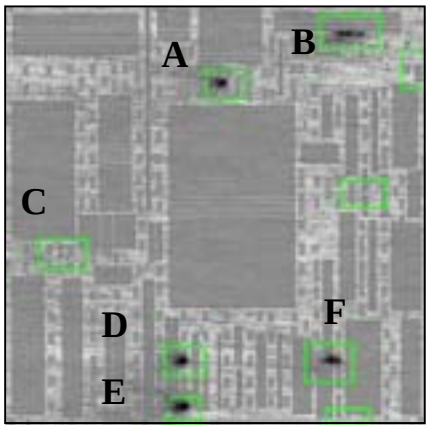

Figure 5: TIVA results at electrical overload sites imaged by SSM in fig. 4a.

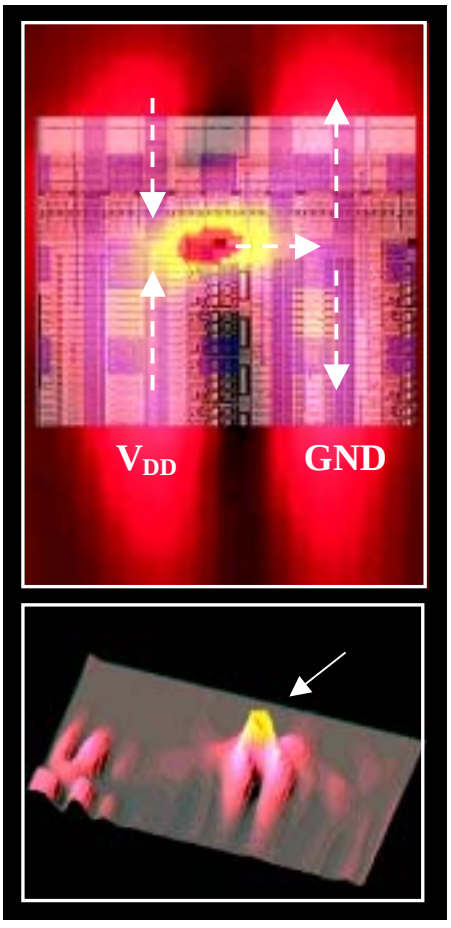

Figure 6: a) Magnified SSM image of fig. 4a site 'B', overlaid with CAD layout. Arrows indicate current paths. Vertical Vdd and GND traces are separated by about 540 microns. b) Surface plot of same site.

ASIC Reliability Stress Failure

A 0.1 micron L-drawn, 9 mm square ASIC product with six levels of metal, failing for power supply shorts, was examined from the backside of a flip-chip CBGA package. The sample was biased with power and ground at 250 $mVAC_{pp}$ and drew 6.5mA (P_{avg} = 800 μW) in a surface mounted socket on a tester interface card. The SSM signal is shown overlaid on a backside optical image in Figure 7. Corresponding STM data with the sample biased at 400 mV and 100 mA are shown in Figure 8 for comparison. Figure 9 shows the magnetic flux density from which the signal highlighted in Fig. 7b is derived.

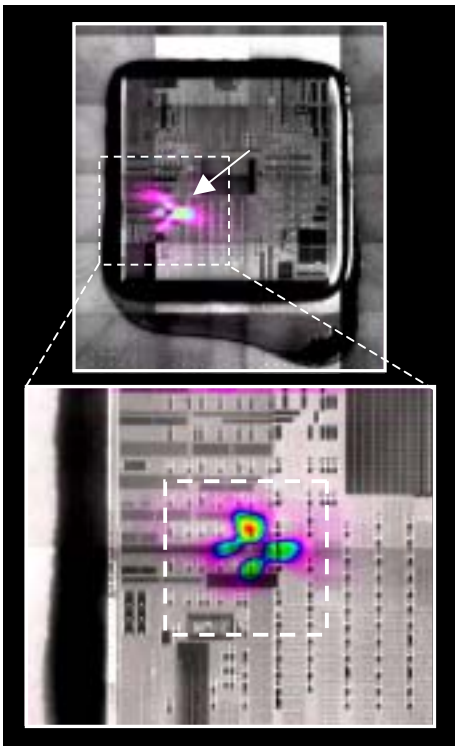

Figure 7: a) SSM signal at shorted site on 9mm-square ASIC. b) Magnified SSM.

Figure 8: STM signal at area highlighted in fig. 7.

Optical examination of the frontside of the chip, after removal from the substrate, identified a defect located at the center of the four-lobed peak highlighted by SSM, and also between the two lobes of the STM signal therein, as seen in Figure 10 (after the images were aligned and scaled using CAD data having features common to all three). A SEM cross-sectional image, seen in Figure 11, confirms considerable damage and short-circuiting underneath the defect site consistent with the concentrated magnetic field indicated by SSM and the strong thermal gradient measured by STM.

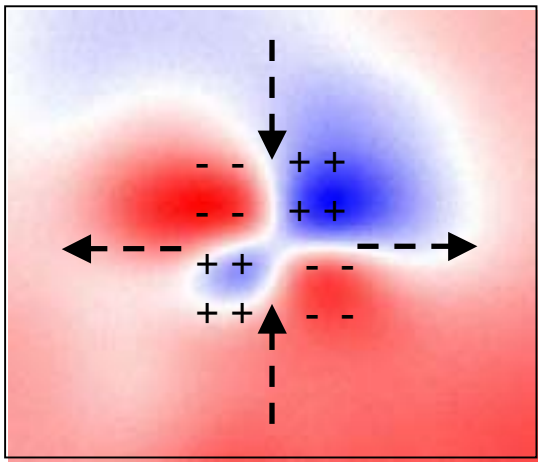

Figure 9: Magnetic flux density and polarity around SSM signal shown in figure 7b. Arrows indicate current flow based on right-hand rule, and consistent with layout in Fig. 10a.

Microprocessor Yield Failure

A power supply short in a 16 x 19 mm, seven level metal, 0.14 micron L-drawn SOI microprocessor was analyzed with SSM from the frontside of the die (frontside liquid crystal had failed to localize a site). The purpose was to examine the spatial resolution attainable from the front side of a device, whereby the SQUID-to-current path distance could be reduced significantly versus scanning from the backside. Power and ground were supplied by two orbital microprobes with a bias of 50 $mVAC_{pp}$ at 1.3 mA (P_{avg} = 31.8 μW). Figure 12 shows the current density and optical overlay with a suspect short circuit location highlighted. Although no defect was found at the site, the surface plot in Figure 13 shows the greater detail gained by frontside (vs. backside) SSM, where scanning distance can be reduced to under 100-microns. Current in the vertical top-metal power busses feeding the defect is clearly visible in both images. More importantly, horizontal paths are also seen, indicating current in a lower interconnect level.

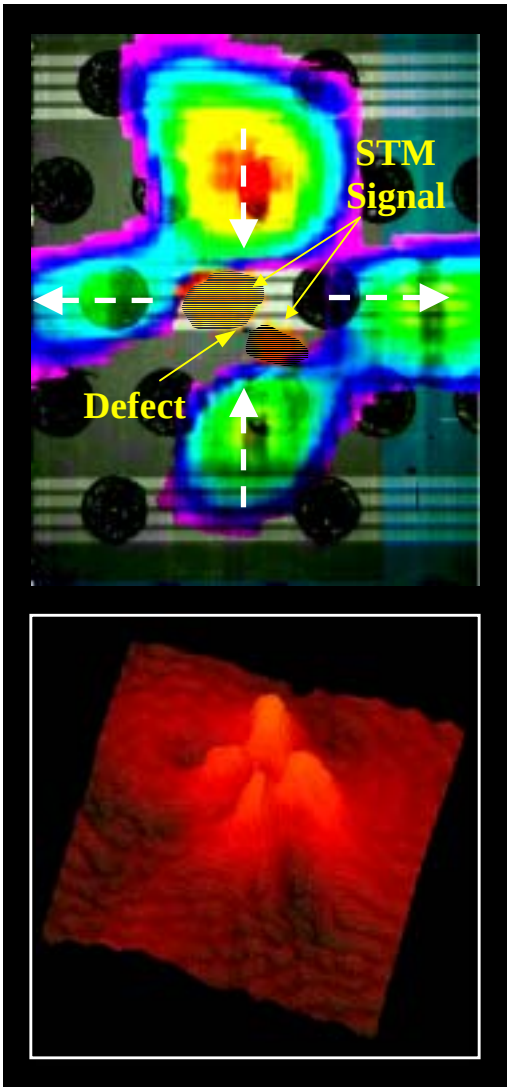

Figure 10: a) Combined SSM, STM, and optical images at site of power supply short circuit. Dashed arrows show direction of current consistent with fig. 9. Vertical scale is approximately 1400 microns. b) Surface plot of SSM signal.

Figure 11: SEM cross-sectional image of shorting site identified in fig.'s 7-10.

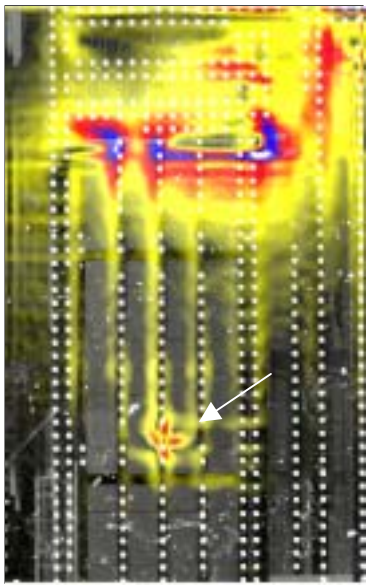

Figure 12: Frontside SSM image of current density on major portion of a 16x19 mm microprocessor.

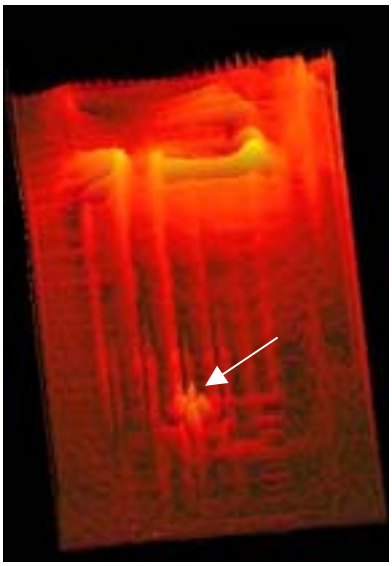

Figure 13: Surface plot of SSM signal in fig. 12.

Discussion

The data presented clearly show that SSM can detect magnetic field gradients and create corresponding current density images caused by short circuits at die level. Strong signals associated particularly with point-source defects are readily apparent and were verified by alternative PFI methods and/or physical failure analysis.

Two distinct signatures are also evident in the data. The single strong peak and surrounding 'fingers' in Fig. 6, for example, are consistent with current converging to and diverging from a point between two conductors. The size scale and orientation of the signature is also in agreement with the circuit layout shown in Fig, 6a. A second signature, the four-lobed signal in Fig.'s 7, 9, and 10, is also consistent qualitatively and dimensionally with current converging and diverging on orthogonal paths. The polarity of the magnetic flux in Fig, 9 was used to determine the direction of current. The flux concentration in this case is caused by the superposition of the gradients associated with the four current segments. Contributing to the four-lobed nature of the signature is the physically vertical component of the path seen in Fig, 11. A magnetically 'silent' area exists directly over such vertical segments because their corresponding magnetic flux is parallel to the horizontal SQUID, and therefore not detected by it.

The ultimate precision and accuracy with which current density can be localized by SSM is determined primarily by SQUID spatial resolution, and to a lesser extent by optical image resolution, and overlay accuracy. SQUID spatial resolution is in turn dependent on separation distance, step size, current, and magnetic field noise [13]. Fig, 4b, for example, shows how a peak can be thresholded to one pixel of 20 x 25 microns, limited in this case by the step size chosen. This dimension is also in the range of the limiting SQUID resolution, governed by its size of approximately 30 microns square. As SQUID-to-sample scanning distance is such a strong determinant of resolution, scanning devices from the frontside surface, where possible, is superior as demonstrated by the increased detail shown in Fig, 13, where scanning distance was less than 100 microns.

In comparison with alternative fault isolation techniques, the data show that SSM is qualitatively in good agreement with LC, PEM, STM, and TIVA. While SSM currently suffers in relative spatial resolution it does possess three major advantages. The first is its high sensitivity to current-induced magnetic flux, independent of voltage bias. This enables imaging particularly of very low resistance short circuits often manifested as large area defects. Such failures cause little Joule-heating, may be difficult to heat sufficiently with a laser (e.g., for TIVA), and are difficult to bias at levels sufficient to produce photon emission.

Secondly, the SSM's wide dynamic range allows simultaneous imaging at both relatively low and high current densities. In some cases this rich dataset is an advantage over the more typical highly localized signals often produced by other PFI methods. Finally, the ability to measure magnetic flux through the non-ferrous materials commonly used in ICs, especially in packaging,

broadens the applicability of SSM considerably and enables truly non-destructive analysis.

Conclusions

This paper has shown the efficacy of die level SSM and how it complements alternative PFI techniques. Current density signatures have also been observed which correlate well with expected results based on knowledge of circuit layout and expected direction of current in the failing samples.

A number of developments in SSM technology would enhance its performance in die level fault isolation. Improved optical spatial resolution coupled with a peak- fitting algorithm would enhance the ultimate precision and accuracy of defect localization. Development of a so-called X-oriented SQUID (i.e., an orientation in which the plane of the SQUID is normal to the chip surface) would improve raw spatial resolution, as would a smaller diameter Z-SQUID (albeit sacrificing sensitivity in the latter case). Early experiments using lock-in synchronization with functional test patterns to improve signal to noise ratio have been promising and need to be continued. Lastly, modeling of magnetic fields and their current density signatures, validated by physical failure analysis, could enable expanded signature analysis and improve overall diagnosis time and efficiency.

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