Proceedings from the 30th International Symposium for Testing and Failure Analysis,
November 14-18, 2004 Worcester, Massachusetts

Failure Analysis of Short Faults on Advanced Wire-bond and Flip-chip Packages with Scanning SQUID Microscopy

Steve K. Hsiung, Kevan V. Tan, Andrew J. Komrowski, Daniel J. D. Sullivan
LSI Logic Corporation, 3098 West Warren Avenue, Fremont, California 94539
Tel: 408-433-8838 Fax: 408-433-8892 Email: stevehs@lsil.com

Jan Gaudestad
Neocera, Inc., 10000 Virginia Manor Road, Beltsville, Maryland 20705
Tel: 301-210-1010 Fax: 301-210-1042 Email: gaudestad@neocera.com

Abstract

Scanning SQUID (Superconducting Quantum Interference Device) Microscopy, known as SSM, is a non-destructive technique that detects magnetic fields in Integrated Circuits (IC). The magnetic field, when converted to current density via Fast Fourier Transform (FFT), is particularly useful to detect shorts and high resistance (HR) defects. A short between two wires or layers will cause the current to diverge from the path the designer intended. An analyst can see where the current is not matching the design, thereby easily localizing the fault. Many defects occur between or under metal layers that make it impossible using visible light or infrared emission detecting equipment to locate the defect. SSM is the only tool that can detect signals from defects under metal layers, since magnetic fields are not affected by them. New analysis software makes it possible for the analyst to overlay design layouts, such as CAD Knights, directly onto the current paths found by the SSM.

In this paper, we present four case studies where SSM successfully localized short faults in advanced wire-bond and flip-chip packages after other fault analysis methods failed to locate the defects.

Introduction

SQUID (Superconducting Quantum Interference Device) is the most sensitive magnetic field detector currently known. In recent years, current imaging through magnetic field detection using a SQUID sensor has become a mainstream approach for short localization in the package [1]. The technique is also utilized for die level applications [2]. Magnetic fields are not blocked by typical package and semiconductor materials such as package molding compounds, heat sinks, metal layers or silicon. The device can therefore be examined non-destructively.

The magnetic field strength scales with current magnitude and decreases with separation between the sensor and source currents. The rate of decrease depends on the nature of the current source, but for ICs the magnetic-field strength is typically inversely proportional to the distance between the sensor and the source [3].

The MAGMA-C20 (Figure 1) is a commercial magnetic field imaging microscope designed for failure analysis of ICs, packages, and boards. It employs a high-temperature SQUID that is cooled down to 77 K. The microscope keeps the SQUID cold and in vacuum, while the DUT is at room temperature in air. The SQUID can be positioned as close as 50 µm from the DUT. Resolution of the system is ±3 µm when the distance from the SQUID to the current carrying structure is about 250 µm or less. The system has a sensitivity of 20 picotesla, or two million times smaller than the Earth's magnetic field, making it sensitive enough to detect currents as small as 10 nA at a 100 µm working distance with 1 second averaging.

The SQUID sensor is oriented parallel to the plane of the sample and is therefore only sensitive to the Z-component of the magnetic field (the component perpendicular to the scanning plane). The SQUID is held stationary while the DUT is raster scanned under the magnetic sensor in a non-contact mode to acquire the magnetic field image. The current supplied to the DUT is typically alternating at a frequency less than 20 kHz. By using a lock-in technique, an image of just the supplied current can be acquired while static background fields are ignored, enabling the system to work in an unshielded environment. The interpretation of the magnetic field image is difficult so a Fast Fourier Transform (FFT) back-evolution technique is used to transform the magnetic field image into an equivalent current image of the integrated circuit or packaged device [3, 4]. The resulting current map can then be compared to a circuit diagram or optical/IR image to determine the fault location.

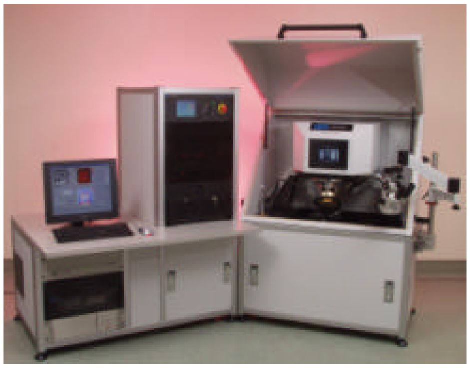

Figure 1 Magma-C20 Scanning SQUID Microscope (SSM)

The basic steps of SSM analysis used on advanced wire-bond and flip-chip packages fall into five categories:

- Sample Preparation
- Scanning
- Data Analysis
- Fault Localization
- Fault Validation

Advanced Wire-bond Packages

Advanced wire-bond packages, unlike traditional Ball Grid Array (BGA) packages, have multiple pad rows on the die and multiple tiers on the substrate (Figure 2 and Figure 3). The advanced wire-bond packages at LSI Logic have high pin count and small die size employing LSI Logic's Gflx Cu/Low-K process and Pad-on-IO wire bonding.

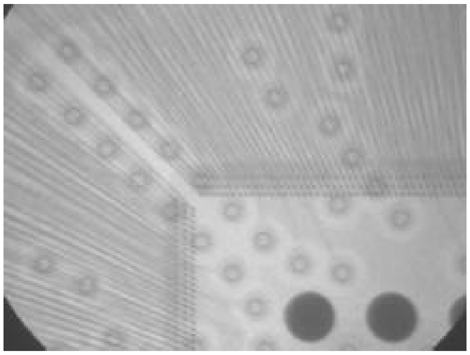

Figure 2 X-ray image of an advanced wire-bond package

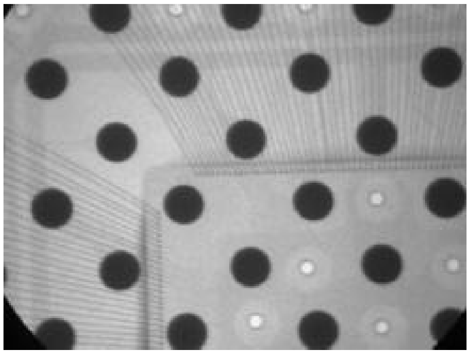

Figure 3 X-ray image of a traditional wire-bond package

This package technology has brought new challenges to failure analysis. To date, Scanning Acoustic Microscopy (SAM), Time Domain Reflectometry (TDR) analysis, and Real-Time X-ray (RTX) inspection were the non-destructive tools used to detect short faults. Unfortunately, these techniques do not work very well in advanced wire-bond packages: SAM is used to detect anomalies at die and package interfaces; TDR can only tell if the short occurs on die side or substrate. Most importantly, because of the high-density wire bonding in advanced wire-bond packages, it is extremely hard to localize the short with conventional RTX inspection.

Without detailed information as to where the short might occur, attempting destructive decapsualtion to expose both die surface and bond wires is full of risk. Wet chemical etching to remove mold compound in a large area often results in overetching. Furthermore, even if the package is successfully decapped, visual inspection of the multi-tiered bond wires is a blind search.

SSM analysis, however, provides an alternative and new non-destructive approach to localize short faults.

Sample Preparation

To improve the resolution of the SSM images, cursory sample preparation is necessary. On wire bond packages, the mold cap needs to be thinned as much as possible. Typically it is lapped down to the top of the bond wire loop without contacting the bond wires. This allows the SQUID sensor to be rastered closely to the sample surface, while ensuring the device retains electrical functionality.

Scanning

Wires are soldered to the solder balls of a DUT. The device is then put on the stage in the probe station of SSM. An AC voltage is applied to the device proportional to the current of the short fault. If the device is packaged with a daisy-chain die, given the resistance between the shorted pins, the voltage applied should make the current less than 2 μA. Each scan takes about forty-five minutes to one hour depending on scanning area and image resolution.

Data Analysis

The SSM data are current density images and current peak images. The current density images give the magnitude of the current, while the current peak images reveal the current path with a ± 3 µm resolution.

Obtaining the SSM data from scanning advanced wire-bond packages is only half the task; fault localization is still necessary. The critical step is to overlay the SSM current images or current path images with CAD files such as bonding diagrams or RTX images to pinpoint the fault location.

To make alignment of overlaying possible, an optical two-point reference alignment is made. The package edge and package fiducial are the most convenient package markings to align to.

Fault Localization

Based on the data analysis, fault localization by SSM should isolate the short in the die, bond wires or package substrate.

Fault Validation

After all non-destructive approaches are exhausted, the final step is destructive deprocessing to verify SSM data. Depending on fault isolation, the deprocessing techniques include decapsulation, parallel lapping or cross-section.

Case Study I

One advanced wire-bond package device failed with a short between two I/O pins. TDR analysis characterized the short to beyond the bare substrate (i.e. the bond wires), but RTX inspection did not show any anomalies.

The device was then analyzed by SSM. The SSM current density image (Figure 4) and current peak image (Figure 5) were obtained. The current density image was then overlaid to the bonding diagram (Figure 6). The short is on the die side (Figure 7).

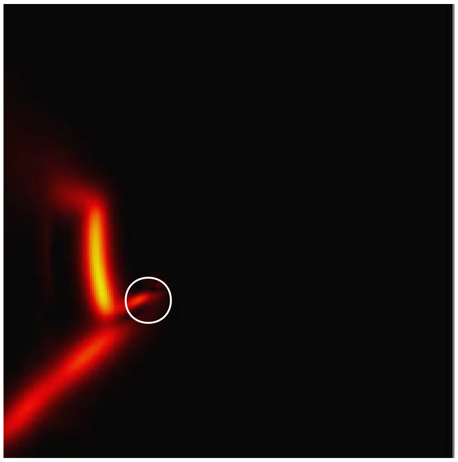

Figure 4 SSM current density image

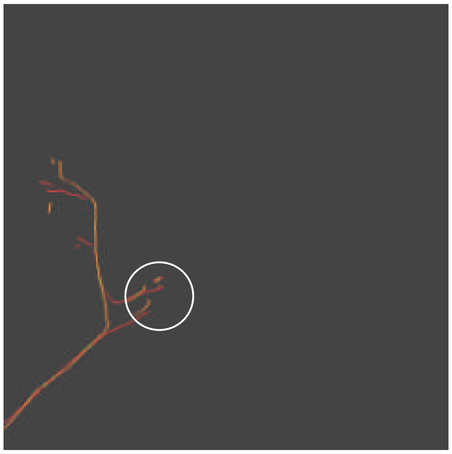

Figure 5 SSM current peak image

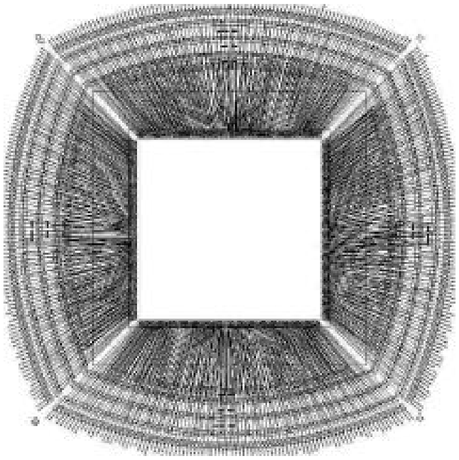

Figure 6 CAD file of the bonding diagram

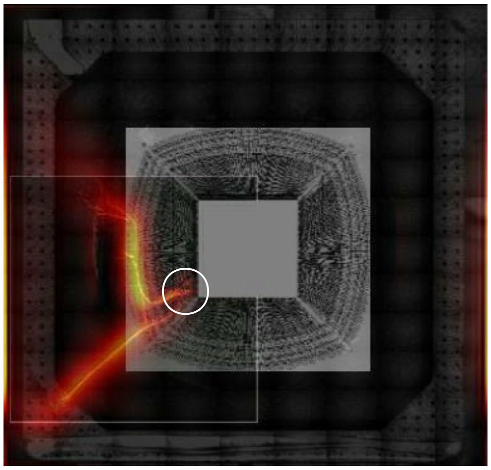

Figure 7 SSM current density image overlaying CAD file

The device was then chemically decapped on the die surface. Visual inspection revealed a partially lifted ball bond from one failing I/O pin contacting the bond wire of the other failing I/O pin (Figure 8). The short went away after the ball bond was pushed away.

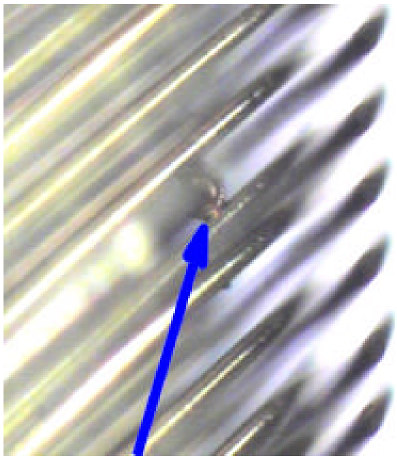

Figure 8 Optical image of the lifted ball bond of one failing I/O pin that was touching the bond wire of the other failing I/O pin

Case Study II

One advanced wire-bond package device failed with a short between I/O and VSS. TDR analysis showed that the short was again beyond the bare substrate. Again, RTX inspection did not show any anomalies.

The SSM current peak image (Figure 9) overlaid with the bonding diagram pinpointed the short to bond wires close to the power ring (Figure 10).

Chemical decapsulation to expose bond wires is risky, because it often results in overetching. Employing a laser ablation tool, the mold compound was selectively removed at the target area, exposing the entire bond wire loop (Figure 11).

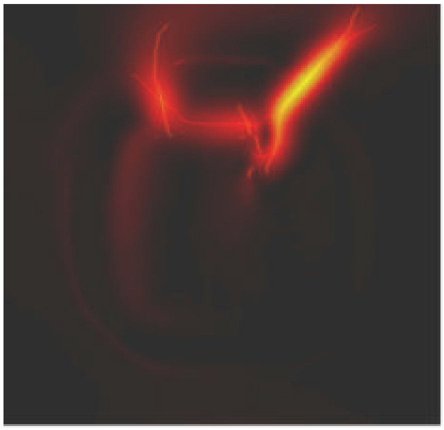

Figure 9 SSM current density/peak image

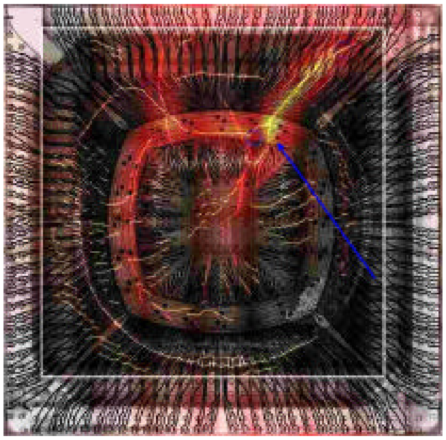

Figure 10 SSM current peak image overlaid with bonding diagram pinpoints short to bond wires close to the power ring

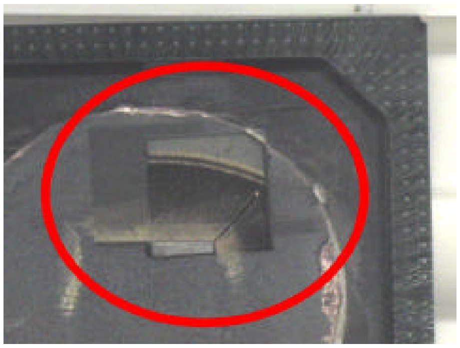

Figure 11 Optical image of the device where mold compound was partially removed by a laser decapsulation tool

Based on SSM data, visual inspection was focused at the VSS power ring. Two bond wires were observed to be shorting close to the power ring (Figure 12). The short disappeared after the two bond wires were separated.

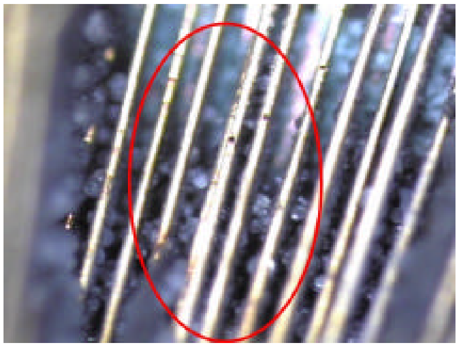

Figure 12 Optical image of two shorted bond wires in the area indicated by SSM data

Flip-chip Packages

Until recently, localizing power short fault in the core area of LSI Logic's flip-chip packages with non-destructive methods was challenging. TDR analysis does not apply for power shorts. The most common technique was to separate the die from the substrate and perform random inspection through parallel-lap of the substrate. Given the large area of the power core (Figure 13), most of the time searching without localization was in vain.

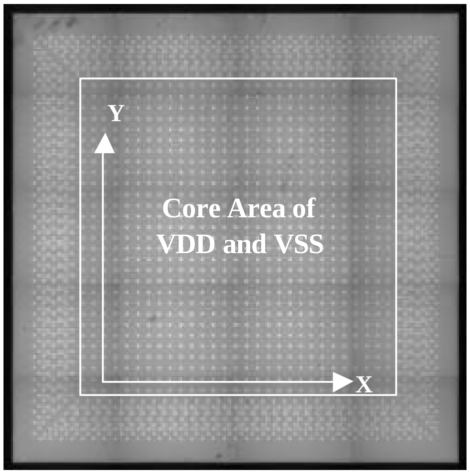

Figure 13 IR image of a core area of VDD and VSS where X-Y position is marked

With SSM analysis it is possible to localize the X-Y position of short faults in the core. More importantly, Z-position information is available. This makes possible distinguishing shorts in the interconnect solder bumps from shorts in the package substrate (Figure 14).

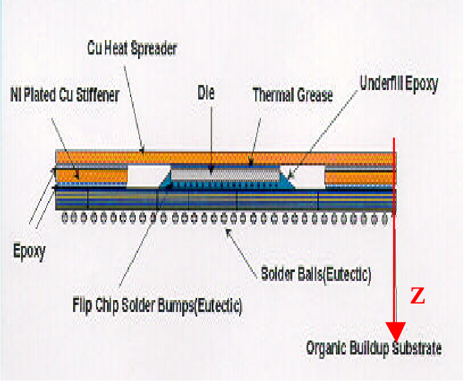

Figure 14 Schematic of Z position of die, interconnect solder bumps and substrate in flip-chip packages

Sample Preparation

For flip-chip packages, the bulk silicon needs to be thinned down to about 100 µm. The die backside surface is polished and covered by an anti-reflective coating material to obtain better infrared images (Figure 15).

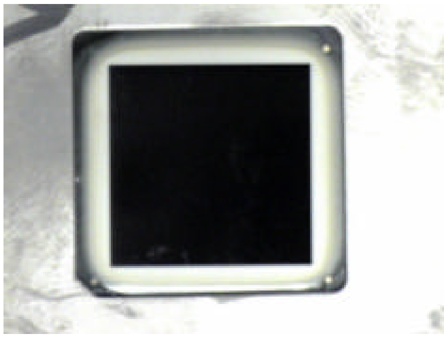

Figure 15 Optical image of a die backside after the die is thinned down to 100µm and the die backside surface is covered by an anti-reflective coating material

Scanning

To protect short defects from fusing open, an AC voltage is applied to the devices such that the current is less than 2 µA. Our studies have shown that short faults in the substrate may blow out if the current is above 2 µA for this defect.

There are four SSM and camera images that can be obtained from flip-chip packages: current density images, peak images, optical/Infra Red (IR) images and static magnetic field images. The procedures to localize short faults in X-Y-Z position may include four steps:

Step 1 Power up VDD and VSS pins. Then perform SSM to see if there is a spot with strong current density.

Step 2 Power up different VDD and VSS pins. Then perform SSM to see if there are other spots with strong current density.

Step 3 Power up all VDD pins and perform SSM. This helps distinguish the current features in the VDD plane.

Step 4 Power up all VSS pins and make a scan. This helps distinguish the current features in the VSS plane.

Data Analysis

In flip-chip packages optical/IR images, AC magnetic field images, current density images, current peak images and DC static magnetic field images are acquired together.

Data analysis on the DC magnetic field images also yields magnetic dipoles. This information is useful because a static magnetic dipole suggests a magnetic material is present.

Fault Localization

After overlaying current density images to optical/IR images, if the spots with strong current density in **Step 1** and **Step 2** are the same, then that is the X-Y position of the short fault.

To isolate the Z-position of the short fault, the images gained from **Step 3** and **Step 4** will be compared to the CAD files of the substrate drawings. The images obtained in **Step 1** and **Step 2** are then compared to the images obtained in **Step 3** and **Step 4** and to the substrate drawings, to find which layer the current passes through to get to the shorted location. If the images match the substrate drawings, then it indicates the short occurs in the substrate.

Fault Validation

Based on data analysis on X-Y-Z positions of a short fault, die removal by mechanical grinding is the first step for fault validation.

If the short is localized in interconnect solder bumps, parallel-lapping in the region of the current density peak will expose the anomaly.

If the short fault is isolated to the package substrate, plasma ashing to remove underfill material followed by electric probing confirms the SSM data. Then, based on Z-position of short fault, the substrate is parallel-lapped, and inspected sequentially to identify the root cause.

Case Study III

One flip-chip package with daisy-chain die failed power short between VDD Core and VSS Core. The resistance between the two power domains was 7.8 Ohms. Acoustic Microscopy in C-Mode (C-SAM) did not find any delamination or void. RTX and IR inspections did not observe any bridging between solder bumps.

Two VDD pins on top left and right corners and two VSS pins on bottom left and right corners were connected. The current was set less than 2 µA. The device was scanned. The SSM current density image overlaid IR image shows a spot with strong current density (Figure 16).

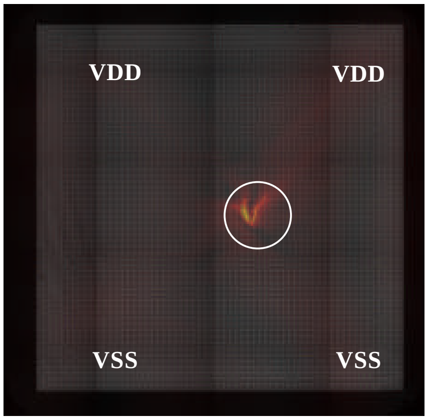

Figure 16 SSM current density image overlaid IR image shows a spot with strong current density using one set of VDD and VSS pins

Next, two different VDD pins and two different VSS pins were connected. The device was scanned again. The SSM current image overlaid IR image pinpoints to the same location with strong current density (Figure 17).

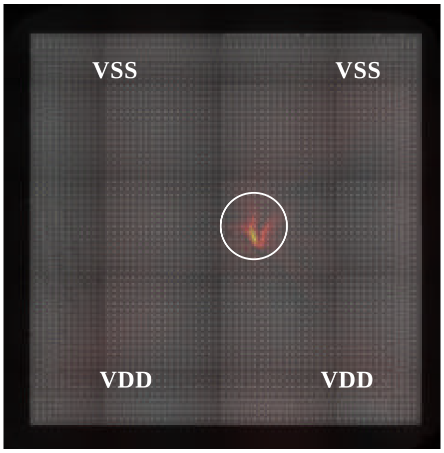

Figure 17 SSM current density image overlaid IR image shows a spot with strong current density when powered by a different set of VDD and VSS pins

The DC static magnetic field image revealed a dipole in that spot that suggests there might be a magnetic material such as Iron, Nickel or Cobalt at this location (Figure 18).

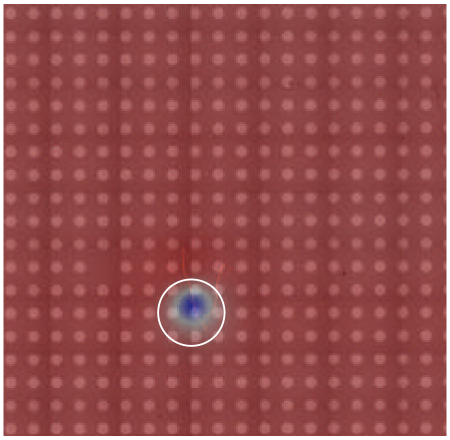

Figure 18 SSM peak current image overlaid DC static magnetic field image revealed a magnetic dipole in that spot

The current peak image overlaid with the IR image in high resolution indicates the short fault is in interconnect solder bumps, not in the package substrate. This is identified by tracing the current path; the current is observed to be closer to the surface in the region of the short than the current flow in other parts of the package (the current density peak is largest close to the SQUID sensor). This yields the Z-position of the fault.

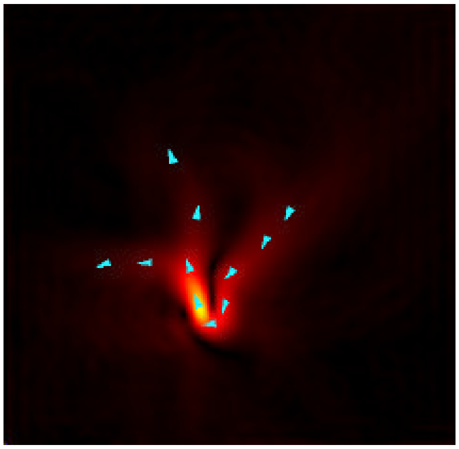

Figure 19 The SSM current peak image in high resolution indicates the short is in the interconnect solder bumps

The die was removed by mechanical grinding. Visual inspection revealed an anomaly at the location identified by SSM (Figure 20). Parallel-lapping the solder bumps revealed a particle trapped between solder bumps of VDD and VSS in the underfill material (Figure 21). EDX analysis identified the particle to be composed of Fe (Iron), Ni (Nickel) and Cr (Chromium) (Figure 22). The stainless steel particle confirms the SSM data analysis.

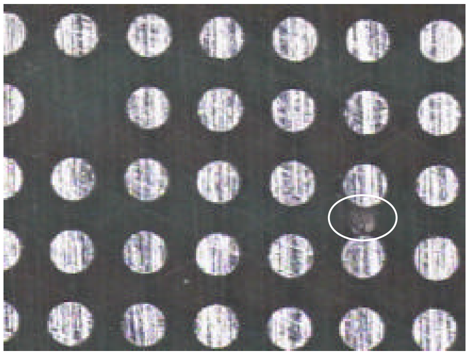

Figure 20 Optical image of an anomaly in the location identified by the SSM

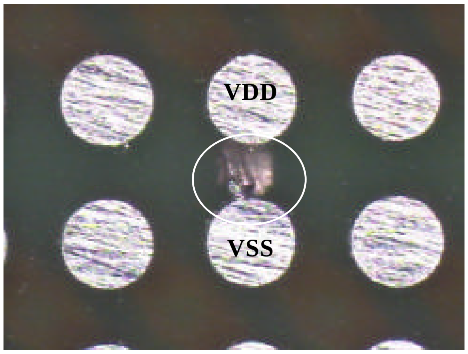

Figure 21 Optical image of a particle trapped between solder bumps of VDD Core and VSS Core in underfill material

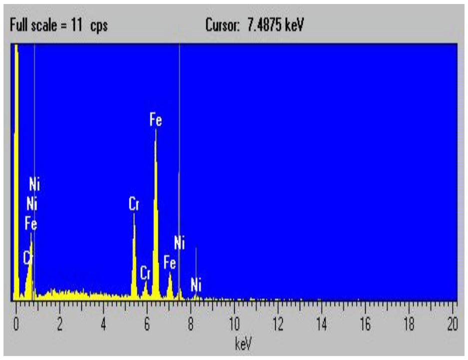

Figure 22 EDX spectrum of the particle that shows the elements of Fe (Iron), Ni (Nickel) and Cr (chromium)

Case Study IV

One flip-chip device failed with a power short in the core area. The resistance between power domains was 1.7 KΩ. After GSAM analysis, RTX and IR inspections did not reveal any anomalies, the device was then analyzed by SSM.

The first scan was taken with a VDD pin on top left corner and a VSS pin on bottom center connected. The second scan was done with a VDD pin on top right corner and a VSS pin on center left connected. The current was set less than 2 μA. Both scans generated images with strong current density at the same location (Figure 23 and Figure 24). This is the X-Y position of the short fault.

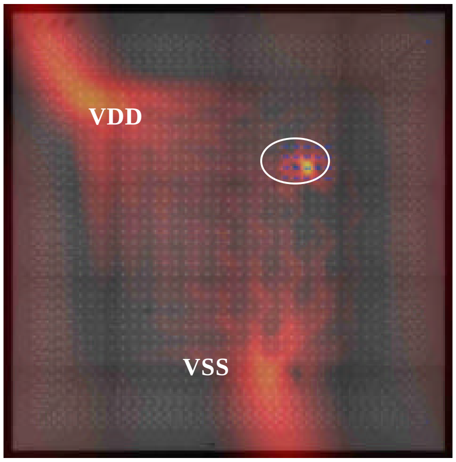

Figure 23 SSM current density image overlaid IR image shows a location with strong current density

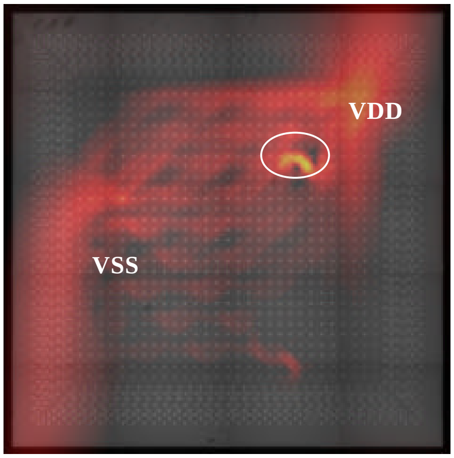

Figure 24 SSM current density image overlaid IR image shows the same location with strong current density even when different VDD and VSS pins were connected

The current density image overlaid IR image in high resolution did not show very obvious sign of the Z-position of the fault. The current density was diffuse. There was also no magnetic dipole observed in that location (Figure 25).

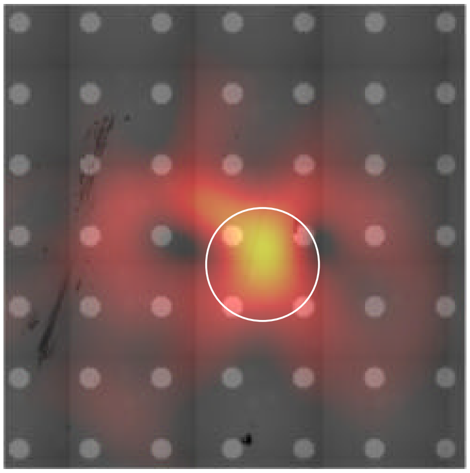

Figure 25 SSM current density image overlaid IR image in high resolution

To locate the Z-position, **Step 3** and **Step 4** mentioned before were taken. The images were then compared with CAD file of the substrate drawing. The data suggest that the fault is in the 1st and 2nd layer of the substrate.

After the die was removed by mechanical grinding (Figure 26) and the underfill material was removed by plasma ashing (Figure 27), the resistance remained the same at 1.7 KΩ. This confirms the SSM data analysis -- the short occurred in the package substrate. A defect was found at the location identified by SSM in the substrate after sequential parallel-lapping and cross-section.

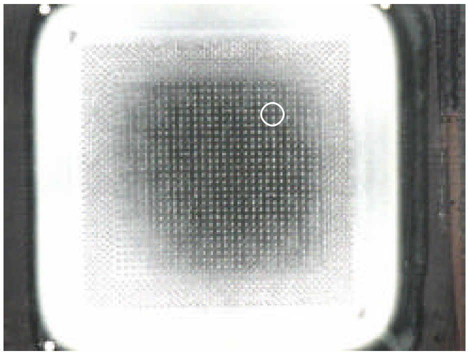

Figure 26 Optical image of the device after die was removed by mechanical grinding

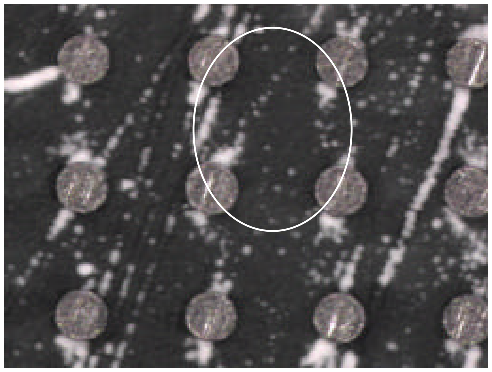

Figure 27 Optical image in high resolution of the location after underfill material was dissolved by plasma ashing

Conclusion

Our case studies employing Scanning SQUID Microscopy in advanced wire-bond and flip-chip packages demonstrate its capability as a novel and non-destructive failure analysis tool to isolate short faults at low current levels (2μA or less). In each case study, fault validation verified the accuracy of SSM in localizing the X-Y position of the root defect, and in case study III, the Z position was also verified. The SSM technique has been proven to be successful in situations where SAM, TDR and X-ray are not successful.

Acknowledgements

The authors would like to thank their colleagues at LSI Logic and Neocera for their support in the failure analysis of these parts and the development of this technique. The authors would also like to thank Sameer Patel, who made great contributions to the results.

References

[1] Dias, R. et al, “Integration of SQUID Microscopy into FA Flow”, Proceedings of 2001 ISTFA, pp.77-81

[2] Vallett, D. et al, “Scanning SQUID Microscopy for Die Level Fault Isolation”, Proceedings of 2002 ISTFA, pp.391-396

[3] Chatraphorn, et. Al., “Scanning SQUID Microscopy of Integrated Circuits”, Applied Physics Letters; 76 (16): 2304 (2004)

[4] Wikswo, Jr. JP. The Magnetic Inverse Problem for NDE”, in Weinstock H (ed.). SQUID Sensors: Fundamentals, Fabrication, and Applications. The Netherlands: Kluwer Academic Publishers; 1996, pp. 629-695

[5] Fleet EF, et al, “HTS Scanning SQUID Microscopy of Active Circuits”, IEEE Transactions on Applied Superconductivity 1999; 9(2): 4103

[6] Hsiung, S. et al, “Failure Analysis on Resistive Opens with Scanning SQUID Microscopy”, Proceedings of 2004 International Reliability Physics Symposium, pp. 611

[6] Mai, Z. et al, “Short Failure Analysis under Fault Isolation”, Proceedings of 2001 International Testing and Failure Analysis Symposium, pp.202